

WHAT IS CLAIMED IS:

- 1 1. A semiconductor die package comprising:
2 a semiconductor die comprising a vertical power transistor, wherein the
3 semiconductor die has a first surface and a second surface;
4 a source region at the first surface of the semiconductor die;
5 a gate at the first surface of the semiconductor die;
6 a drain region at the second surface of the semiconductor die;
7 a ground plane proximate the second surface and distal to the first surface; and
8 a bus member covering a portion the first surface of the semiconductor die and
9 having at least one leg, wherein the bus member electrically couples the source region of the
10 semiconductor die to the ground plane.
- 1 2. The semiconductor die package of claim 1 wherein the vertical power
2 transistor is a vertical diffused metal oxide semiconductor (VDMOS).
- 1 3. The semiconductor die package of claim 1 further comprising:
2 an isolator layer between the ground plane and the semiconductor die.
- 1 4. The semiconductor die package of claim 1 further comprising:
2 an isolator layer between the ground plane and the semiconductor die; and
3 a conductive layer between the isolator layer and the semiconductor die.
- 1 5. The semiconductor die package of claim 1 further comprising:
2 an isolator layer between the ground plane and the semiconductor die;
3 a conductive layer between the isolator layer and the semiconductor die; and
4 a ceramic carrier enclosing the semiconductor die, the bus member, the
5 isolator layer, and the conductive layer.
- 1 6. The semiconductor die package of claim 1 wherein the vertical power
2 transistor is a vertical diffused metal oxide semiconductor (VDMOS) RF power transistor.
- 1 7. The semiconductor die package of claim 1 further comprising:
2 an isolator layer between the ground plane and the semiconductor die;
3 a conductive layer between the isolator layer and the semiconductor die;

4 a ceramic carrier enclosing the semiconductor die, the bus member, the
5 isolator layer, and the conductive layer;
6 a drain lead passing through the ceramic carrier;
7 a first wire coupling the drain lead to the drain region via the conductive layer;
8 a gate lead passing through the ceramic carrier; and
9 a second wire coupling the gate lead to the gate.

1 8. The semiconductor die package of claim 1 further comprising a
2 matching network electrically coupled to the gate.

1 9. The semiconductor die package of claim 1 further comprising:
2 an isolator layer between the ground plane and the semiconductor die;
3 a matching network on the isolator layer;
4 a conductive layer between the isolator layer and the semiconductor die;
5 a ceramic carrier enclosing the semiconductor die, the bus member, the
6 isolator layer, and the conductive layer;
7 a drain lead passing through the ceramic carrier;
8 a first wire coupling the drain lead to the drain region via the conductive layer;
9 a gate lead passing through the ceramic carrier;
0 a second wire coupling the gate lead to the matching network; and
1 a third wire coupling the gate to the matching network.

1 10. The semiconductor die of claim 1 wherein gate is a trenched gate.

1 11. A semiconductor die package comprising:
2 a semiconductor die comprising a vertical power transistor, wherein the
3 semiconductor die has a first surface and a second surface;
4 a source region at the first surface of the semiconductor die;
5 a gate at the first surface of the semiconductor die;
6 a drain region at the second surface of the semiconductor die;
7 a ground plane proximate the second surface and distal to the first surface;
8 a conductive layer between the ground plane and the semiconductor die;
9 an isolator layer disposed between the conductive layer and the ground plane;
10 a bus member covering a major portion of the first surface of the
11 semiconductor die and electrically coupling the source region of the semiconductor die to the
12 ground plane;
13 a carrier enclosing the semiconductor die and the bus member;
14 a drain lead passing through the carrier;
15 a first electrical conductor coupling the drain lead to the conductive layer and
16 the drain region;
17 a gate lead passing through the carrier; and
18 a second electrical conductor coupling the gate lead to the gate.

1 12. The semiconductor die package of claim 11 wherein the bus member is
2 a first bus member and wherein the first electrical conductor is a second bus member and the
3 second electrical conductor is a third bus member, wherein the second and third bus members
4 each have a pair of legs with different lengths.

1 13. The semiconductor die package of claim 11 wherein the vertical power
2 transistor is a vertical diffused metal oxide semiconductor (VDMOS) RF power transistor.

1 14. The semiconductor die package of claim 11 further comprising:
2 a matching network coupled to the gate.

1 15. The semiconductor die of claim 11 wherein the bus member is a first
2 bus member and wherein the first electrical conductor is a second bus member and the second
3 electrical conductor is a third bus member, and wherein the first, second, and third bus
4 members each have a horizontal portion and two legs that are perpendicular to the horizontal
5 portion.

1 16. A semiconductor die package comprising:
2 a semiconductor die comprising a vertical power transistor, wherein the
3 semiconductor die has a first surface and a second surface;
4 an emitter region at the first surface of the semiconductor die;
5 a base region at the first surface of the semiconductor die;
6 a collector region at the second surface of the semiconductor die;
7 a ground plane proximate the second surface and distal to the first surface; and
8 a bus member covering a portion the first surface of the semiconductor die and
9 having at least one leg, wherein the bus member electrically couples the source region of the
10 semiconductor die to the ground plane.

1 17. The semiconductor die package of claim 16 wherein the bus member
2 comprises two legs of substantially equal length.

1 18. A semiconductor die package comprising:
2 a semiconductor die comprising a transistor, wherein the semiconductor die
3 has a first surface and a second surface;
4 a source region in the semiconductor die;
5 a gate in the semiconductor die;
6 a drain region in the semiconductor die;
7 a ground plane proximate the second surface and distal to the first surface; and
8 a bus member covering a portion the first surface of the semiconductor die and
9 having at least one leg, wherein the bus member electrically couples the source region of the
10 semiconductor die to the ground plane.

1 19. The semiconductor die package of claim 18 wherein the source region,
2 the gate, and the drain region are at the first surface of the semiconductor die.